Abstract

Synchronous integrated memory

An output circuit (OUT) can be activated via an activation input (AKT), in the activated state starts an output process for data (D) to be read out, in synchronism with the first internal clock (CLKI1), and outputs the data (D) with a specific phase shift (ΔTOUT) with respect to the first internal clock (CLKI1), in synchronism with the external clock (CLKE), at a data connection (P). A counting unit (CT) starts a counting process for recording the number of successively following first levels of the first internal clock (CLKI1) as soon as a second internal clock (CLKI2), which is synchronized to the external clock (CLKE), for the first time assumes a first level while an output control signal (PAR) is at first level. It activates the output circuit (OUT) as soon as the number of successively following first levels of the first internal clock (CLKI1) has reached a predetermined value.

Figure 1